CLAIMS

What is claimed is:

1. A circuit for setting a substrate voltage level comprising:
   a. means for maintaining a substrate at a first predetermined voltage level;
   b. means for maintaining the substrate at a second predetermined voltage level, wherein the second predetermined voltage level is higher than the first predetermined voltage level;
   c. means for maintaining the substrate at a third predetermined voltage level, wherein the third predetermined voltage level is lower than the first predetermined voltage level.

2. The circuit according to claim 1 further comprising means for selecting between the first predetermined level, the second predetermined level and the third predetermined level.

3. The circuit according to claim 1 further comprising:
   a. means for maintaining the substrate at a fourth predetermined voltage level, wherein the fourth predetermined voltage level is higher than the second predetermined voltage level; and
   b. means for maintaining the substrate at a fifth predetermined voltage level, wherein the fifth predetermined voltage level is lower than the third predetermined voltage level.

4. The circuit according to claim 3 further comprising means for selecting between the first predetermined level, the second predetermined level, the third predetermined level, the fourth predetermined level and the fifth predetermined level.

5. A circuit for setting a substrate voltage level comprising:

a. a plurality of resistive elements coupled to each other in a series to form a chain of resistive elements, the chain having a first terminal and a second terminal;

b. a reference voltage source coupled to the first terminal;

c. a substrate coupled to the second terminal; and

d. a plurality of switches wherein each switch is coupled to bypass at least one of the resistive elements.

6. The circuit according to claim 5 wherein the resistive elements each have non-linear resistances.

7. The circuit according to claim 5 wherein the resistive elements comprise diodes.

8. The circuit according to claim 5 wherein the resistive elements comprise MOSFETs.

9. The circuit according to claim 5 wherein the switches comprise MOSFETs.

10. The circuit according to claim 5 further comprising a charge pump coupled to control the substrate voltage level.

11. A circuit for setting a substrate voltage level comprising:

a. a first n-channel MOSFET having a first gate, a first drain and a first source wherein the first gate is coupled to the first drain and the first gate is coupled to a voltage reference level;

b. a second n-channel MOSFET having a second gate, a second drain and a second source wherein the second gate is coupled to the second drain and the second gate is coupled to the first source;

c. a third n-channel MOSFET having a third gate, a third drain and a third source wherein the third gate is coupled to the third drain and the third gate is coupled to the second source;

d. a forth n-channel MOSFET having a forth gate, a forth drain and a forth source wherein the forth gate is coupled to be controlled by a first control voltage and the forth drain is coupled to the third drain and the forth source is coupled to the third source;

e. a fifth n-channel MOSFET having a fifth gate, a fifth drain and a fifth source wherein the fifth gate is coupled to the third gate and the fifth drain is coupled to the third source and the fifth source is coupled to a substrate; and

f. a sixth n-channel MOSFET having a sixth gate, a sixth drain and a sixth source wherein the sixth drain is coupled to the fifth drain and the sixth source is coupled to the fifth source and the sixth gate is coupled to be controlled by a second control voltage.

12. The circuit according to claim 11 further comprising a charge pump having a input terminal and an output terminal, wherein the input terminal is coupled to the first source and the output terminal is coupled to the substrate.

13. The circuit according to claim 11 further comprising:

a. a seventh n-channel MOSFET having a seventh gate, a seventh drain and a seventh source wherein the seventh gate is coupled to the fifth gate, the seventh drain is coupled to the fifth source and the seventh source is coupled to the substrate; and

b. an eighth n-channel MOSFET having an eighth gate, an eighth drain and an eighth source, wherein the eighth gate is coupled to be controlled by a third control voltage level, the eighth drain is coupled to the seventh drain and the eighth source is coupled to the seventh source.

14. The circuit according to claim 13 further comprising a charge pump having a input terminal and an output terminal, wherein the input terminal is coupled to the first source and the output terminal is coupled to the substrate.

15. The circuit according to claim 13 further comprising:

a. a ninth n-channel MOSFET having a ninth gate, a ninth drain and a ninth source wherein the ninth gate is coupled to the seventh gate, the ninth drain is coupled to the seventh source and the ninth source is coupled to the substrate; and

b. a tenth n-channel MOSFET having a tenth gate, a tenth drain and a tenth source, wherein the tenth gate is coupled to be controlled by a forth control voltage level, the tenth drain is coupled to the ninth drain and the tenth source is coupled to the ninth source.

16. The circuit according to claim 15 further comprising a charge pump having a input terminal and an output terminal, wherein the input terminal is coupled to the first source and the output terminal is coupled to the substrate.

17. A method of testing integrated circuit chips comprising the steps of:

a. setting a voltage level of a substrate to a first predetermined level; and

b. setting the voltage level of the substrate to a second predetermined level wherein the second predetermined level is higher than the first predetermined level.

18. A method of testing integrated circuit chips comprising the steps of:

a. setting a voltage level of a substrate to a first predetermined level; and

b. setting the voltage level of the substrate to a second predetermined level wherein the second predetermined level is lower than the first predetermined level.

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